Amendments to the Claims:

Please amend claims 1, 23, 34, 45-47, and 49-51 as follows. Please cancel claims 12-22 and 48. This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (currently amended) A memory module for use in a memory system, the memory module comprising:

a first memory module including a memory device, a first buffer, and a second buffer, the first buffer receiving a first write clock signal and a control signal that includes a read or write command in a first direction of transmission, the second buffer receiving the first write clock signal in the first direction of transmission and a first read clock signal in a second direction of transmission, the second buffer being coupled to a first data bus and a second data bus;

the first memory module generating a second write clock signal in response to, and in phase with, the first write clock signal, for transmitting data from the second buffer in the first direction of transmission if the write command indicates that data is to be written to a second memory module in the memory system, and generating a memory write clock signal in response to, and in phase with, the first write clock signal, for writing data from the second buffer to the memory device if the write command indicates that data is to be written to the memory device in the first memory module; and

the first memory module generating a memory read clock signal in response to, and in phase with, a memory write clock signal, for reading data from the memory device to the second buffer if the read command indicates that data is to be read from the memory device in the first memory module, the memory write clock signal having substantially the same propagation delay as data transferred from the second buffer to the memory device and the memory read clock signal having substantially the same propagation delay as data transferred from the memory device to the second buffer.

2. (previously presented) The memory module of claim 1 wherein the first memory module further generates a second read clock signal in response to, and in phase with, the first write clock signal, for transmitting data from the second buffer in the second direction of transmission.

3. (previously presented) The memory module of claim 1 wherein the memory read clock signal is a clock signal returned from the memory device in response to, and in phase with, the memory write clock signal.

4. (original) The memory module of claim 3 wherein the memory read clock signal is generated on a transmission path that is coupled to a transmission path of the memory write clock signal.

5. (original) The memory module of claim 4 further comprising a dummy load coupled to the transmission path of the memory read clock signal and the memory write clock signal.

6. (previously presented) The memory module of claim 4 wherein the transmission path of the memory read clock signal and the transmission path of the memory write clock signal are substantially equal in length to that of a transmission path of the data between the memory device and the second buffer.

7. (previously presented) The memory module of claim 1 wherein the second write clock signal is generated in response to, and in phase with, the first write clock signal, such that the second write clock signal is transferred to the second memory module.

8. (original) The memory module of claim 7 wherein the second write clock signal is generated by a phase locked loop or delay locked loop on the first memory module in response to the first write clock signal.

9. (previously presented) The memory module of claim 1 wherein the second buffer receives a decoding signal generated at the first buffer to determine whether data access is from the memory device on the first memory module or from a memory device on the second memory module

10. (previously presented) The memory module of claim 1 wherein the first buffer receives a first latency signal and transfers the first latency signal to the memory device in response to the first write clock signal.

11. (original) The memory module of claim 10 wherein the first buffer generates a second latency signal in response to the first latency signal.

12. - 22 (canceled)

23. (currently amended) A memory module for use in a memory system, the memory module comprising:

a first memory module including a memory device and a buffer, the buffer receiving a first write clock signal and a control signal that includes a read or write command in a first direction of transmission, the buffer receiving a first read clock signal in a second direction of transmission, the buffer being coupled to a first data bus and a second data bus; and

the first memory module generating a memory write clock signal in response to, and in phase with, the first write clock signal, for writing data from the buffer to the memory device if the write command indicates that data is to be written to the memory device in the first module, the memory write clock signal having substantially the same propagation delay as data transferred from the buffer to the memory device.

24. (previously presented) The memory module of claim 23 wherein the first memory module generates a second write clock signal in response to, and in phase with, the first write

clock signal, for transmitting data from the buffer in the first direction of transmission if the write command indicates that data is to be written to a second memory module in the memory system.

25. (original) The memory module of claim 24 wherein the second write clock signal is generated by a phase locked loop or delay locked loop on the first memory module in response to the first write clock signal.

26. (previously presented) The memory module of claim 23 wherein the first memory module generates a memory read clock signal in response to, and in phase with, the memory write clock signal, for reading data from the memory device to the buffer if the read command indicates that data is to be read from the memory device in the first memory module.

27. (original) The memory module of claim 26 wherein the memory read clock signal is a clock signal returned from the memory device in response to the memory write clock signal.

28. (original) The memory module of claim 26 further comprising a dummy load coupled to a transmission path of the memory read clock signal and the memory write clock signal.

29. (original) The memory module of claim 26 further comprising a phase locked loop or delay locked loop coupled to a transmission path of the memory read clock signal and the memory write clock signal.

30. (previously presented) The memory module of claim 23 wherein the first memory module generates a second read clock signal in response to, and in phase with, the first write clock signal, for transmitting data from the buffer in the second direction of transmission if the read command indicates that data is to be read from a second memory module in the memory system.

31. (previously presented) The memory module of claim 23 wherein the buffer comprises a first buffer and a second buffer, the second buffer receiving a decoding signal generated at the first buffer to determine whether data access is from the memory device on the first memory module or from a memory device on a second memory module in the memory system.

32. (previously presented) The memory module of claim 31 wherein the first buffer receives a first latency signal and transfers the ~~buffered~~ first latency signal to the memory device in response to the first write clock signal.

33. (previously presented) The memory module of claim 32 wherein the first buffer generates a second latency signal in response to the first latency signal.

34. (currently amended) A memory module for use in a memory system, the memory module comprising:

a first memory module including a memory device and a buffer, the buffer receiving a first write clock signal and a control signal that includes a read or write command in a first direction of transmission, the buffer receiving a first read clock signal in a second direction of transmission, the buffer being coupled to a first data bus and a second data bus; and

the first memory module generating a memory read clock signal in response to, and in phase with, a memory write clock signal, for reading data from the memory device to the buffer if the read command indicates that data is to be read from the memory device in the first memory module the memory read clock signal having substantially the same propagation delay as data transferred from the memory device to the buffer; the memory write clock signal being generated in response to, and in phase with, the first write clock signal.

35. (previously presented) The memory module of claim 34 wherein the first memory module generates a second write clock signal in response to, and in phase with, the first write clock signal, for transmitting data from the buffer in the first direction of transmission if the write command indicates that data is to be written to a second memory module in the memory system.

36. (previously presented) The memory module of claim 34 wherein the first memory module generates a memory write clock signal in response to, and in phase with, the first write clock signal, for writing data from the buffer to the memory device if the write command indicates that data is to be written to the memory device in the first memory module.

37. (previously presented) The memory module of claim 34 wherein the first memory module generates a second read clock signal in response to, and in phase with, the first write clock signal, for transmitting data from the buffer in the second direction of transmission if the read command indicates that data is to be read from a second memory module in the memory system.

38. (previously presented) The memory module of claim 34 wherein the buffer comprises a first buffer and a second buffer, the second buffer receiving a decoding signal generated at the first buffer to determine whether data access is from the memory device on the first memory module or from a memory device on a second memory module in the memory system.

39. (previously presented) The memory module of claim 38 wherein the first buffer receives a first latency signal and transfers the first latency signal to the memory device in response to the first write clock signal.

40. (original) The memory module of claim 39 wherein the first buffer generates a second latency signal in response to the first latency signal.

41. (previously presented) A memory module for use in a memory system, the memory module comprising:

a first memory module including a memory device and a buffer, the buffer receiving a first write clock signal and a control signal that includes a read or write command in a first direction of transmission, the buffer receiving a first read clock signal in a second direction of transmission, the buffer being coupled to a first data bus and a second data bus; and

the first memory module generating a second read clock signal in response to, and in phase with, the first write clock signal, for transmitting data from the buffer in the second direction of transmission if the read command indicates that data is to be read from a second memory module in the memory system.

42. (previously presented) The memory module of claim 41 wherein the first memory module generates a second write clock signal in response to, and in phase with, the first write clock signal, for transmitting data from the buffer in the first direction of transmission if the write command indicates that data is to be written to the second memory module in the memory system.

43. (previously presented) The memory module of claim 41 wherein the first memory module generates a memory write clock signal in response to, and in phase with, the first write clock signal, for writing data from the buffer to the memory device if the write command indicates that data is to be written to the memory device in the first memory module.

44. (previously presented) The memory module of claim 41 wherein the first memory module generates a memory read clock signal in response to, and in phase with, a memory write clock signal for reading data from the memory device to the buffer if the read command indicates that data is to be read from the memory device in the first memory module, the memory write clock signal being generated in response to, and in phase with, the first write clock signal.

45. (currently amended) A memory system comprising:

a memory controller for generating a first write clock signal and a control signal that includes a read or write command; and

a first memory module including a memory device and a buffer, the buffer receiving the first write clock signal and the control signal in a first direction of transmission, the buffer receiving a first read clock signal in a second direction of transmission, the buffer being coupled to a first data bus and a second data bus;

the first memory module generating a second write clock signal in response to, and in phase with, the first write clock signal, for transmitting data from the buffer in the first direction of transmission if the write command indicates that data is to be written to a second memory module in the memory system, and generating a memory write clock signal in response to, and in phase with, the first write clock signal for writing data from the buffer to the memory device if the write command indicates that data is to be written to the memory device in the first memory module; and

the first memory module generating a memory read clock signal in response to, and in phase with, the memory write clock signal for reading data from the memory device to the buffer if the read command indicates that data is to be read from the memory device in the first memory module, the memory write clock signal having substantially the same propagation delay as data transferred from the buffer to the memory device and the memory read clock signal having substantially the same propagation delay as data transferred from the memory device to the buffer.

46. (currently amended) A memory system comprising:

a memory controller for generating a first write clock signal and a control signal that includes a read or write command;

a read clock generator for generating a first read clock signal; and

a first memory module including a memory device and a buffer, the buffer

receiving the first write clock signal and the control signal in a first direction of transmission, the buffer receiving the first read clock signal in a second direction of transmission, the buffer being coupled to a first data bus and a second data bus;

the first memory module generating a second write clock signal in response to, and in phase with, the first write clock signal, for transmitting data from the buffer in the first direction of transmission if the write command indicates that data is to be written to a second memory module in the memory system, and generating a memory write clock signal in response to, and in phase with, the first write clock signal, for writing data from the buffer to the memory device if the write command indicates that data is to be written to the memory device in the first memory module;

the first memory module generating a memory read clock signal in response to, and in phase with, the memory write clock signal, for reading data from the memory to the buffer if the read command indicates that data is to be read from the memory device in the first memory module, the memory write clock signal having substantially the same propagation delay as data transferred from the buffer to the memory device and the memory read clock signal having substantially the same propagation delay as data transferred from the memory device to the buffer; and

the first memory module generating a second read clock signal in response to, and in phase with, the first read clock signal, for transmitting data from the buffer in the second direction of transmission.

47. (currently amended) A method for generating clock signals in a memory system comprising:

receiving, at a first buffer on a first memory module ~~including a memory device~~, a first write clock signal and a control signal that includes a read or write command in a first direction of transmission, the first memory module including a memory device;

receiving, at a second buffer on the first memory module, the first write clock

signal in the first direction of transmission and a first read clock signal in a second direction of transmission, the second buffer being coupled to a first data bus and a second data bus;

generating a second write clock signal in response to, and in phase with, the first write clock signal, for transmitting data from the second buffer in the first direction of transmission if the write command indicates that data is to be written to a second memory module in the memory system, and generating a memory write clock signal in response to, and in phase with, the first write clock signal, for writing data from the second buffer to the memory device if the write command indicates that data is to be written to the memory device in the first memory module; and

generating a memory read clock signal in response to, and in phase with, a memory write clock signal, for reading data from the memory device to the second buffer if the read command indicates that data is to be read from the memory device in the first memory module, the memory write clock signal having substantially the same propagation delay as data transferred from the second buffer to the memory device and the memory read clock signal having substantially the same propagation delay as data transferred from the memory device to the second buffer ~~; the memory write clock signal being generated in response to the first write clock signal~~.

48. (canceled)

49. (currently amended) A method for generating a clock signal in a memory system comprising:

receiving, at a buffer on a first memory module ~~including a memory device~~, a first write clock signal and a control signal that includes a read or write command in a first direction of transmission, the first memory module including a memory device;

receiving a first read clock signal in a second direction of transmission, the buffer being coupled to a first data bus and a second data bus; and

generating a memory write clock signal in response to, and in phase with, the first write clock signal, for writing data from the buffer to the memory device if the write command indicates that data is to be written to the memory device in the first memory module, the memory write clock signal having substantially the same propagation delay as data transferred from the buffer to the memory device.

50. (currently amended) A method for generating a clock signal in a memory system comprising:

receiving, at a buffer on a first memory module, a first write clock signal and a control signal that includes a read or write command in a first direction of transmission, the first memory module including a memory device;

receiving a first read clock signal in a second direction of transmission, the buffer being coupled to a first data bus and a second data bus;

generating, in response to the first write clock signal, a memory write clock signal, the memory write clock signal being in phase with the first write clock signal; and

generating a memory read clock signal in response to, and in phase with, the memory write clock signal, for reading data from the memory device to the buffer if the read command indicates that data is to be read from the memory device in the first memory module, the memory read clock signal having substantially the same propagation delay as data transferred from the memory device to the buffer.

51. (previously presented) A method for generating a clock signal in a memory system comprising:

receiving, at a buffer on a first memory module, a first write clock signal and a control signal that includes a read or write command in a first direction of transmission, the first memory module including a memory device;

receiving a first read clock signal in a second direction of transmission, the buffer being coupled to a first data bus and a second data bus; and

generating a second read clock signal in response to, and in phase with, the first write clock signal, for transmitting data from the buffer in the second direction of transmission if the read command indicates that data is to be read from a second memory module in the memory system.